11. A method, comprising:

identifying a first programming state for a first memory cell;

identifying a second programming state different from the first programming state for a second memory cell; and

concurrently verifying that the first memory cell has been programmed to the first programming state and the second memory cell has been programmed to the second programming state, the concurrently verifying includes sensing a first current from the first memory cell while sensing a second current from the second memory cell.

12. The method of claim **11**, wherein:

the concurrently verifying includes biasing a first bit line connected to the first memory cell to a first bit line voltage while biasing a second bit line connected to the second memory cell to a second bit line voltage different from the first bit line voltage.

13. The method of claim **11**, wherein:

the concurrently verifying includes integrating the first current for a first period of time and integrating the second current for a second period of time greater than the first period of time.

14. The method of claim **12**, wherein:

the concurrently verifying includes electrically coupling a first sense amplifier to the first bit line and electrically coupling a second sense amplifier to the second bit line, the concurrently verifying includes setting a first dynamic node associated with the first sense amplifier to a first voltage and setting a second dynamic node associated with the second sense amplifier to a second voltage different from the first voltage.

15. The method of claim **14**, wherein:

the concurrently verifying includes setting the first dynamic node to the first voltage prior to setting the second dynamic node to the second voltage, the first voltage is greater than the second voltage.

16. The method of claim **12**, wherein:

the first bit line voltage is greater than the second bit line voltage.

17. The method of claim **12**, wherein:

the concurrently verifying includes setting a gate of a first NMOS transistor connected to the first bit line to a first voltage such that the first bit line is biased to the first bit line voltage and setting a gate of a second NMOS transistor connected to the second bit line to a second voltage such that the second bit line is biased to the second bit line voltage.

18. The method of claim **17**, wherein:

the concurrently verifying includes determining the first voltage based on the first programming state and determining the second voltage based on the second programming state.

19. The method of claim **11**, wherein:

the first memory cell and the second memory cell are part of a memory array, the memory array comprises a non-volatile memory that is monolithically formed in one or more physical levels of memory cells having active areas disposed above a silicon substrate.

20. A system, comprising:

a memory array including a first memory cell and a second memory cell; and

a plurality of sense amplifiers configured to identify a first programming state of a plurality of programming states for the first memory cell and identify a second programming state of the plurality of programming states for the second memory cell, the plurality of sense amplifiers configured to bias a first bit line connected to the first memory cell to a first bit line voltage based on the first programming state while a second bit line connected to the second memory cell is biased to a second bit line voltage different from the first bit line voltage based on the second programming state, the plurality of sense amplifiers configured to sense a first current from the first memory cell while the first bit line is biased to the first bit line voltage and sense a second current from the second memory cell while the second bit line is biased to the second bit line voltage.

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